ABSTRACT OF THE DISCLOSURE

In a MIS transistor , the top surfaces of source/drain regions (S/D diffusion layers) formed on a semiconductor substrate 1 are arranged nearer to a gate electrode than a channel plane on the semiconductor substrate, and the top surfaces of the source/drain regions are arranged nearer than the channel plane than the interface between a gate insulator film provided on the upper side of the channel plane and the gate electrode. In this transistor, a groove is selectively formed in the surface of the semiconductor substrate, and a polycrystalline silicon deposited in the groove may be used as a mask to form impurity diffusion layers serving as source/drain regions to laminate and form a gate insulator film of a high dielectric film and a gate electrode. Alternatively, the polycrystalline silicon may be selectively formed to be used as a mask to elevate and form the impurity diffusion layer to laminate and form the gate insulator film and the gate electrode. Thus, it is possible to achieve both of the reduction of the resistance of the S/D diffusion layers and the reduction of the gate parasitic capacitance.